RETAC

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Reconfigurable Testing Accelerator

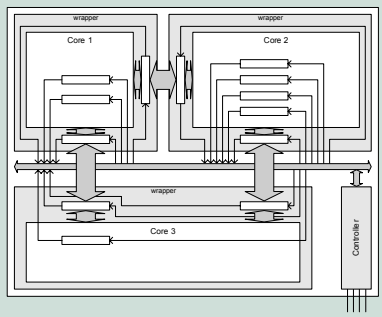
Motivation

- Modern integrated circuits are more susceptible to faults.
- Circuit complexity is increasing, SoC are more often used.
- Testing of circuits is more difficult, more time-consuming and more expensive.

⇓

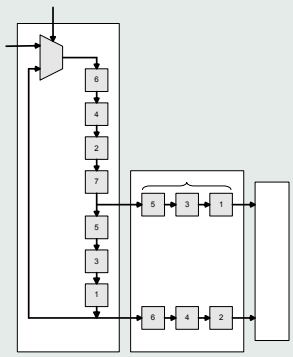
- Use Built-in Self Test Equipment (wrappers, scan chains) and compressed test patterns to reduce cost and time needed for testing.

SoC with BISTE

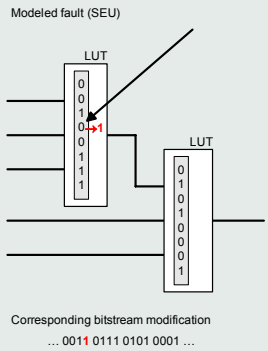


Project Goals

- Create a new technology for diagnosing SoC-type digital circuits – prototype and methodology.
  - Wrappers are based on the RESPIN architecture (IEEE P1500 compliant)
  - Test patterns are compressed using the COMPAS tool
- Speed up fault simulation by utilization of dynamic reconfiguration in FPGA

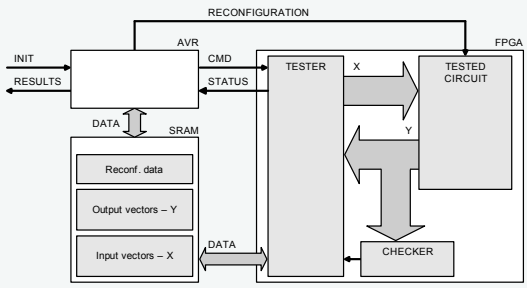


RESPIN architecture

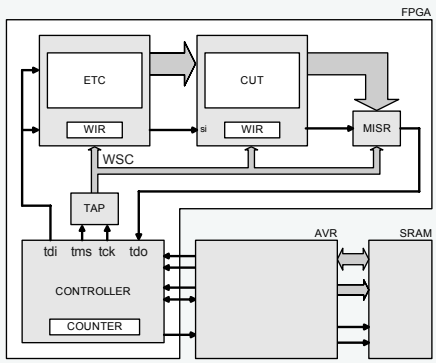


Fault emulation

Results (first 6 months)



HW fault injector in Atmel FPSLIC



Diagnostic system in Atmel FPSLIC

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