The Use of High Temperature Solders in Semiconductor Industry

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Content

- NXP Semiconductors
- Basics of how to Package Semiconductors
- Process of High Pb solder usage
- Materials used in combination with High Pb solder
- Requirements for alternative (Pb-free) compositions
- New Developments

NXP Semiconductors

- Established in 2006
  (formerly a division of Philips)
- Builds on a heritage of
  50+ years of experience in semiconductors
- Provides engineers and designers with semiconductors and software that deliver better sensory experiences
- Top-10 supplier with Sales of € 4.960 Bln (2006)
- Sales: 35% Greater China, 31% Rest of Asia, 25% Europe, 9% North America
- Headquarters: Eindhoven, The Netherlands
- Key focus areas:
  - Mobile & Personal, Home, Automotive & Identification, Multimarket Semiconductors
- Owner of NXP Software: a fully independent software solutions company

Strong customer base

50+ direct customers accounting for approximately 70% of sales

Mobile and Personal

NOKIA, SAMSUNG, LG, Motorola, Apple, Sony Ericsson, BenQ, Ericsson, Cellon, SunCorp, vtech, Siemens, Creative, HP, TechFaithWireless

Home

SHARP, SAMSUNG, Philips, Panasonic, Dell, Sony, BenQ, TCL, AOC, TPV, ASUS, LG, Quanta Computer

Automotive / ID

NOKIA, SAMSUNG, Siemens VDO, Delphi, Visteon, Continental, Bosch, Harman/Becker Automotive Systems, gemalto, Oberthur Card Systems, Bundesdruckerei, Giesecke & Devrient, ACG

Distributors and EMS

Elcoteq, Sanmina-SCI, Foxconn, Avnet, WPG World Peace Group, Jabil, Flextronics, Solectron, Future Electronics, Arrow

IC Manufacturing Operations (IMO Backend)

- Manufacturing base
  - 5 wholly owned assembly & test factories + 3 small European test centers
  - 10000 employees
- Production volume
  - 6 billion products per year, 190 billion pins per year
  - additional 15-20% outsourced

Discrete Manufacturing (IS&O)

- Manufacturing base
  - 3 wholly owned assembly & test factories
  - 4500 employees
- Production volume
  - 42 billion products per year, 125 billion pins per year
  - additional 10% outsourced

IMO assembly and test sites

RF SIP Modules, Bumping

APP3 Cubayao

HVQFN, QFP<100, TSSOP>20, LFBGA

APC Calamba

BGA, QFP, COF, SILP, SDIP

APK Kaoshiung

SO, T/SSOP, DIP, IC-Modules

APB Bangkok

BGA, HVQFN

APS Suzhou

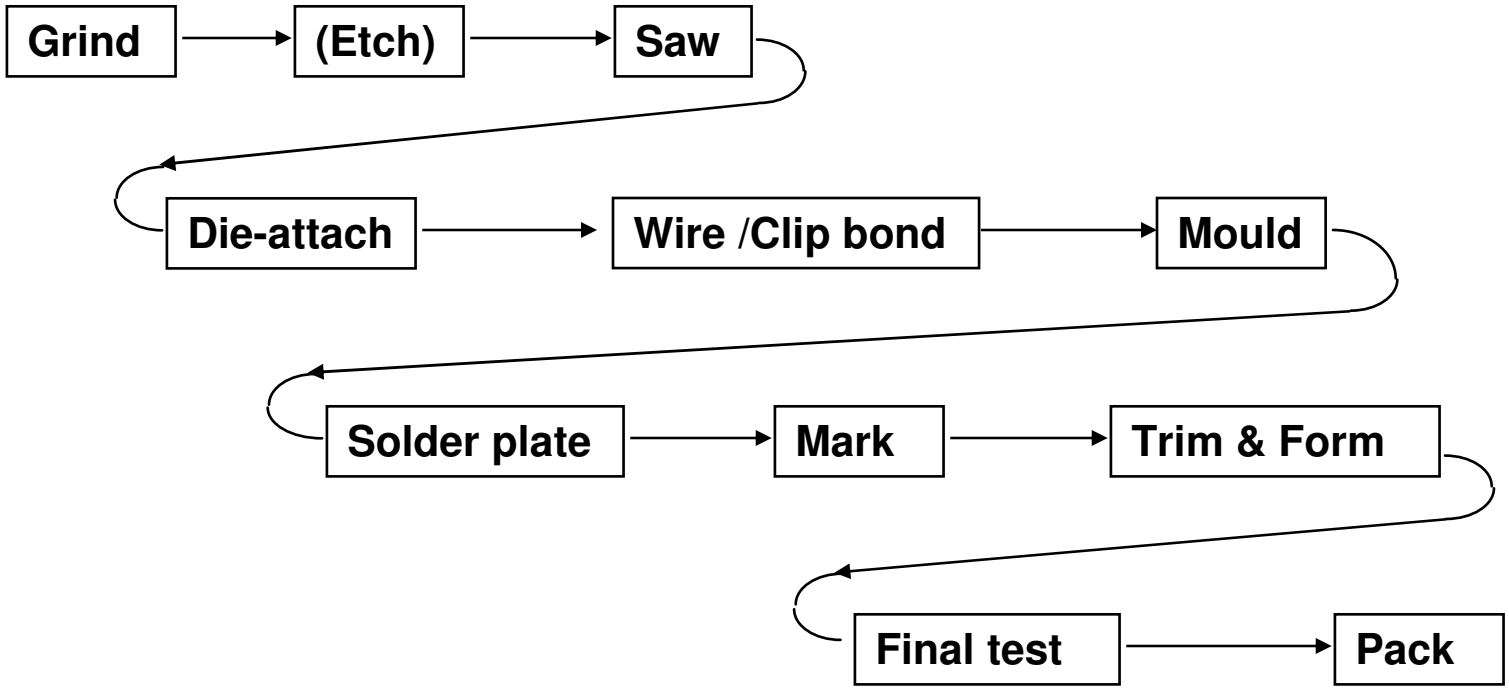
+ 15% outsourcing

- ASE
- Amkor
- NSEB

Basics of how to package semiconductors

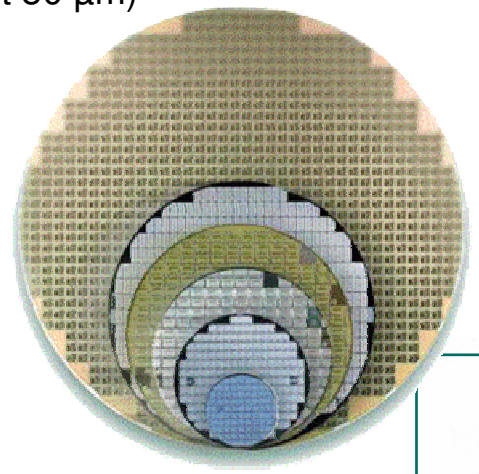
(Back End Process)

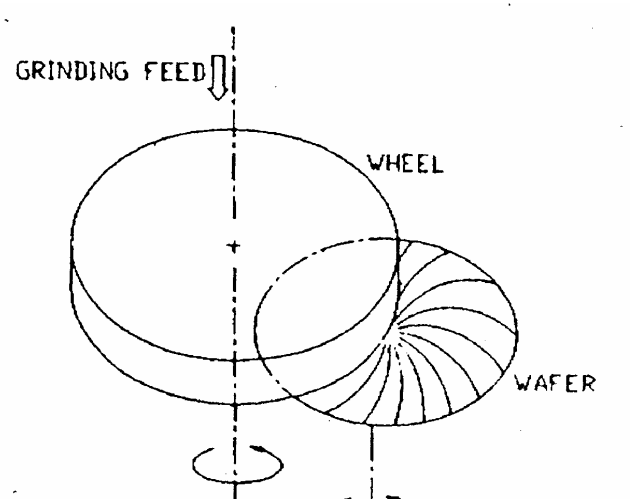
Flowchart (leadframe based packages)



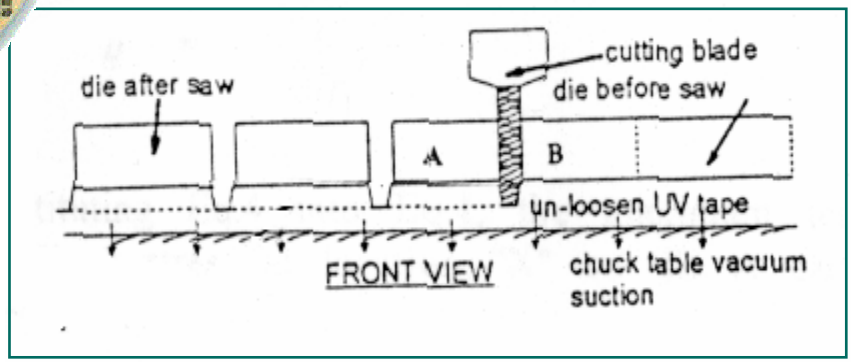
Wafer preparation (Grinding/Etching and Sawing)

- Grinding Process:
  - “in-feed” grinding process
  - additional “back-etch” process
  - standard thickness: 380 µm (280 µm)
  - trend to thin dice (target 50 µm)

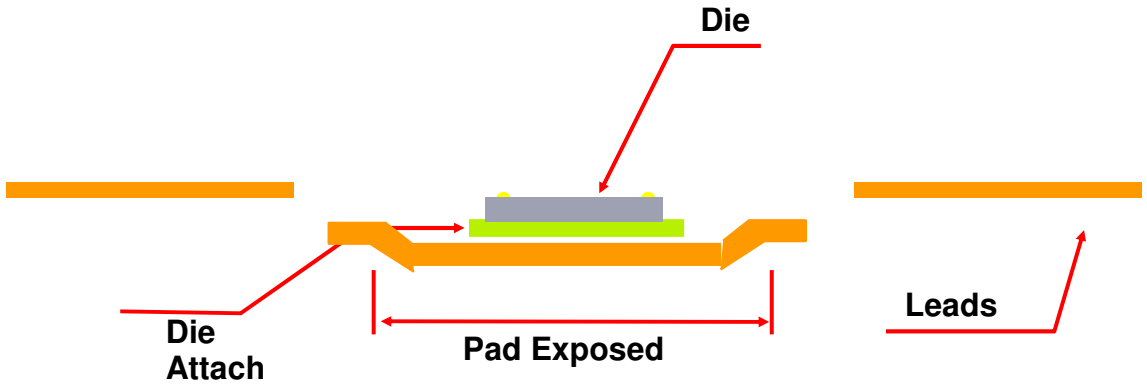




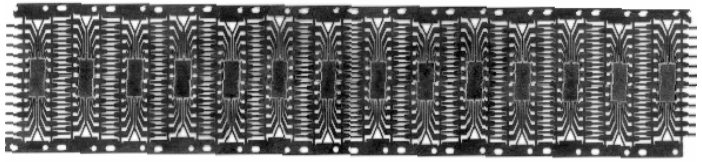
- Sawing Process
  - sawlane width capability (80 to 30 µm)
  - sawing-in-foil



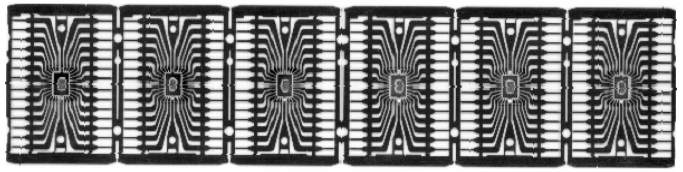
Die-attach



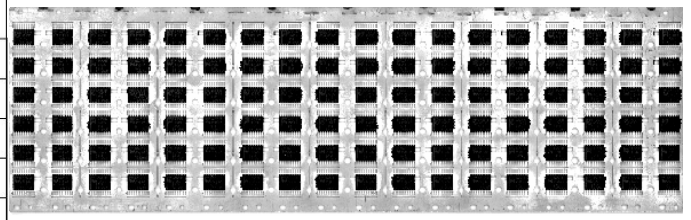
- Function: Connect the Silicon Chip (Die) to Leadframe
- Process:
  - glue: silver filled PI /epoxy = stress / cure
  - Soft solder: discrete/power packages
  - process : stamp transfer / dispensing
  - cure : oven / hotplate



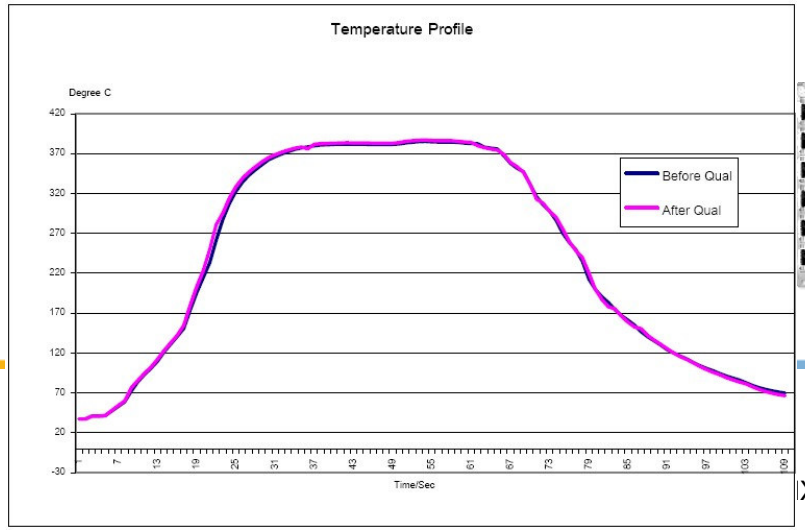
IDF



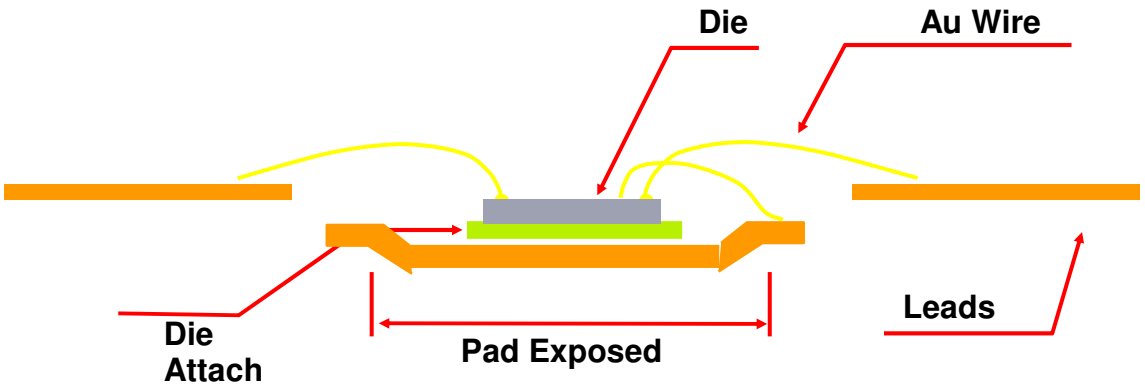
DIP



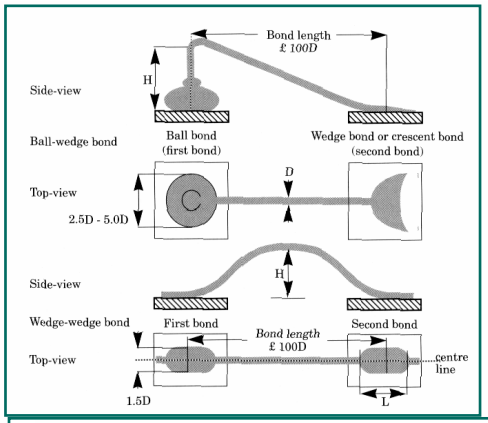
MATRIX (SO)

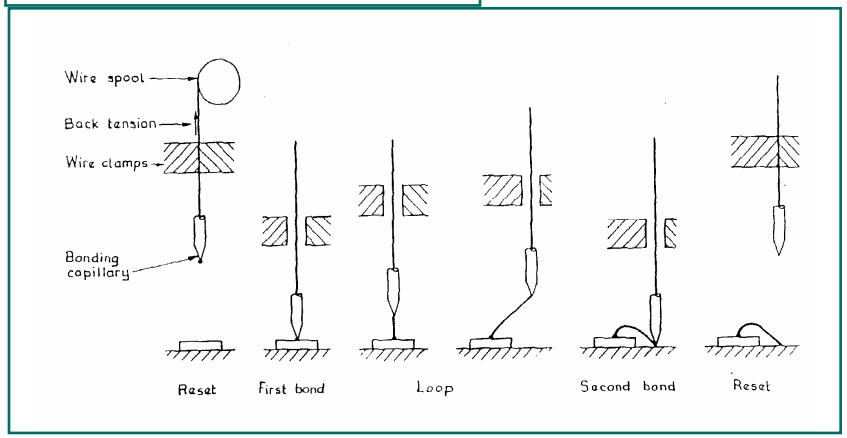


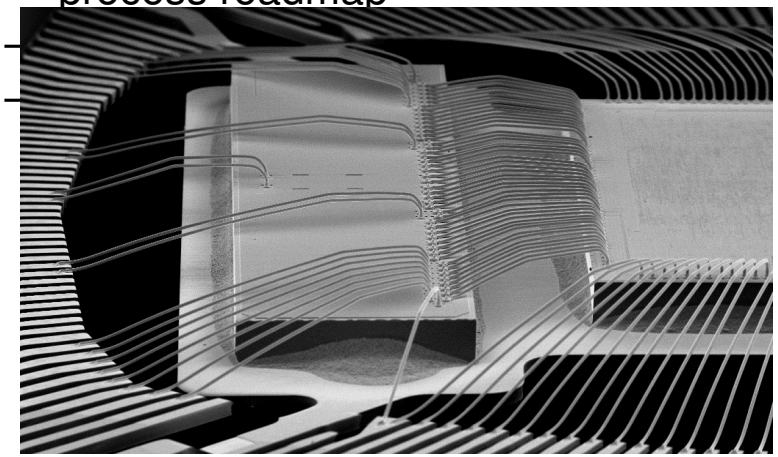
Wirebonding



- Function: Connect chip to leadframefingers
- Process:
  - ball-wedge process (Au-wires, plastic)
  - wedge-wedge process (Al-wires, ceramic)
  - bondpad / bondpad-pitch design rules
  - process roadmap

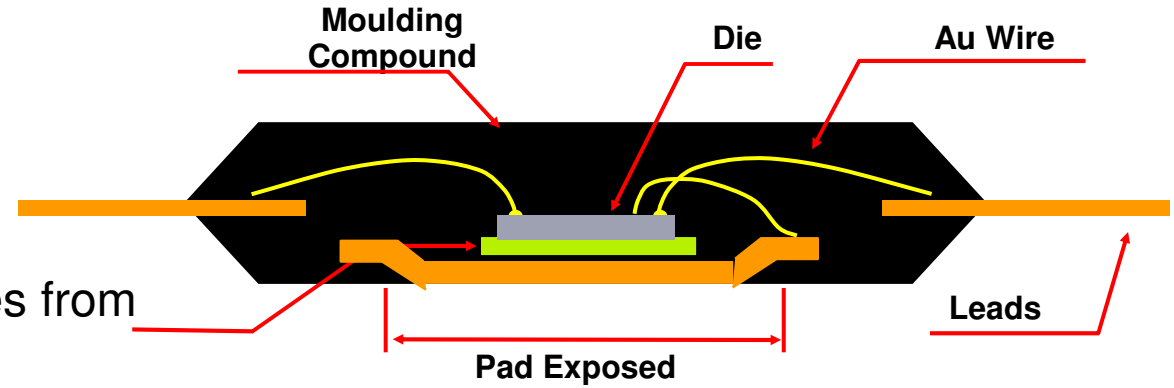






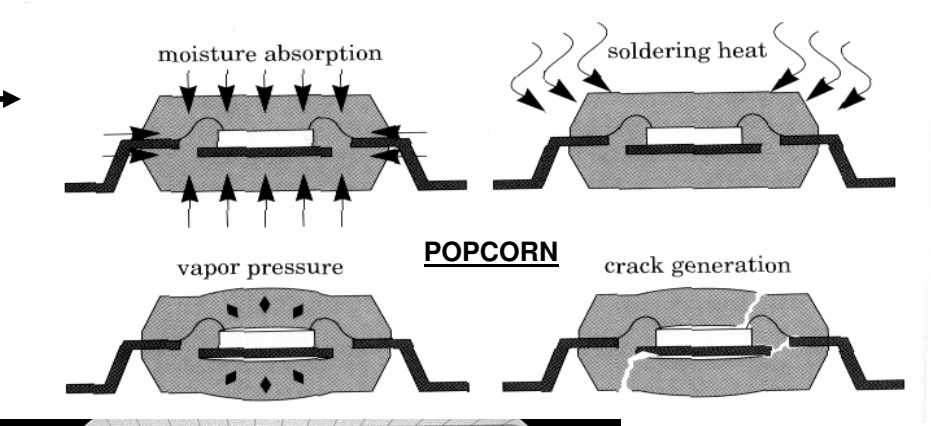
wire bond movie

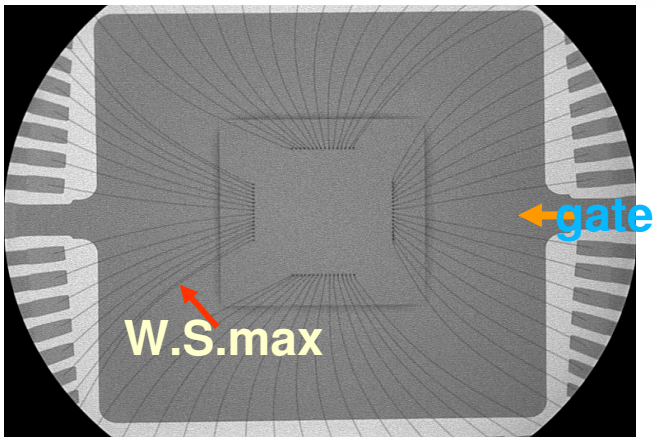
Moulding



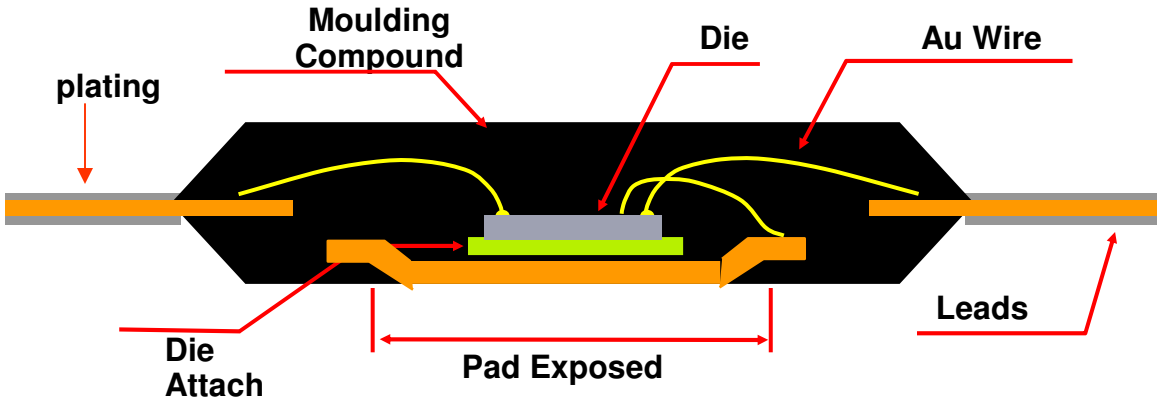
Function: protect the chip/wires from outside influences

- Process / materials:
  - transfer moulding
  - conventional / multiplunjer systems
  - thermo-setting materials
    - standard / low stress / anti-popcorn
- Quality:
  - product reliability:
    - HTSL (ball bond degradation)
    - MSL (moisture sensitivity level MSL=1 is good; MSL=6 is bad / delamination
  - wire-sweep
  - glueability on PCB



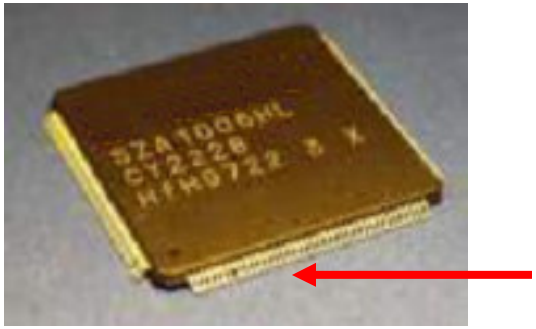


Plating and marking



Plating Process:

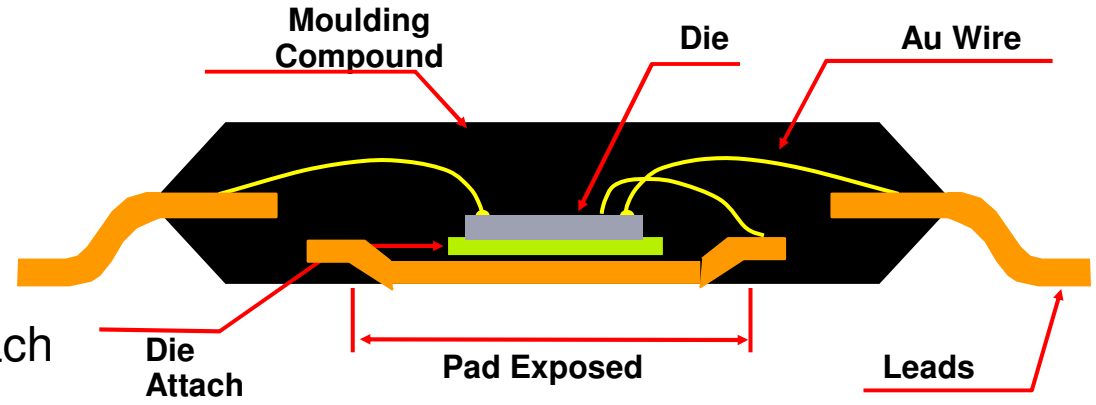
- Function: ensure that package can connect to outside world (can be soldered)
  - Electroplating composition
    - Ni/Pd/Au (preplate)
    - Matte Sn



Marking:

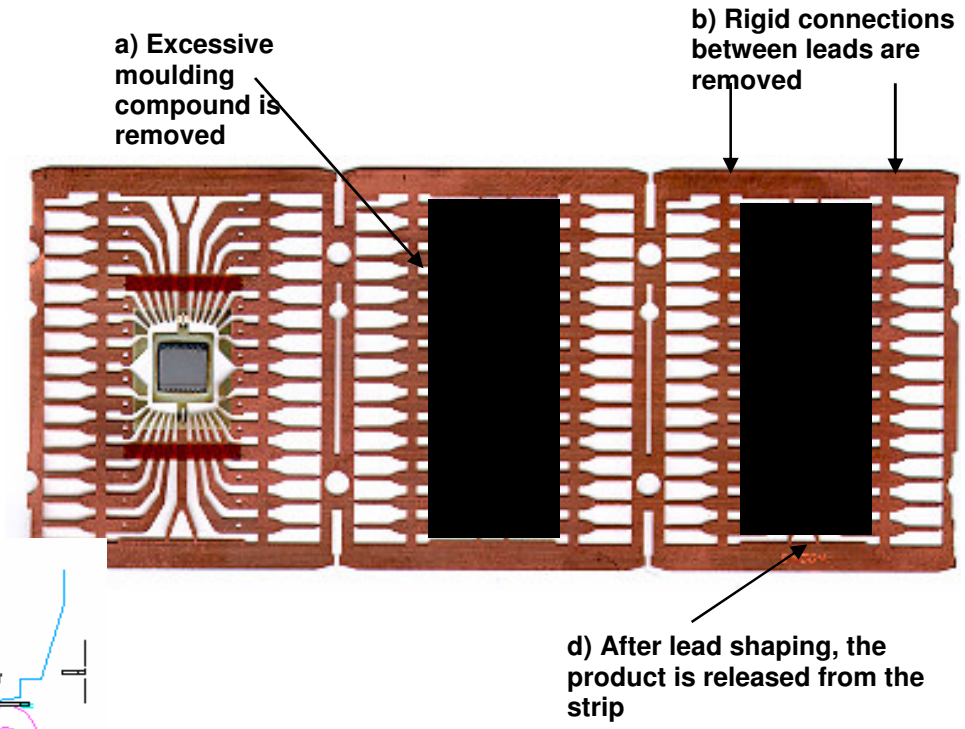
- Ensure identification for traceability
  - Lasermark

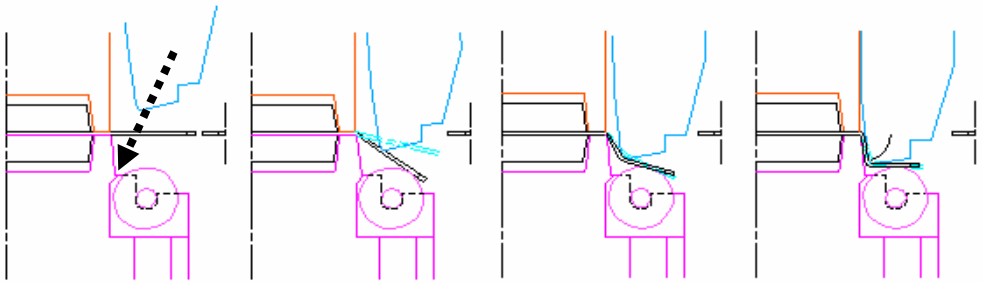
Trim/Form



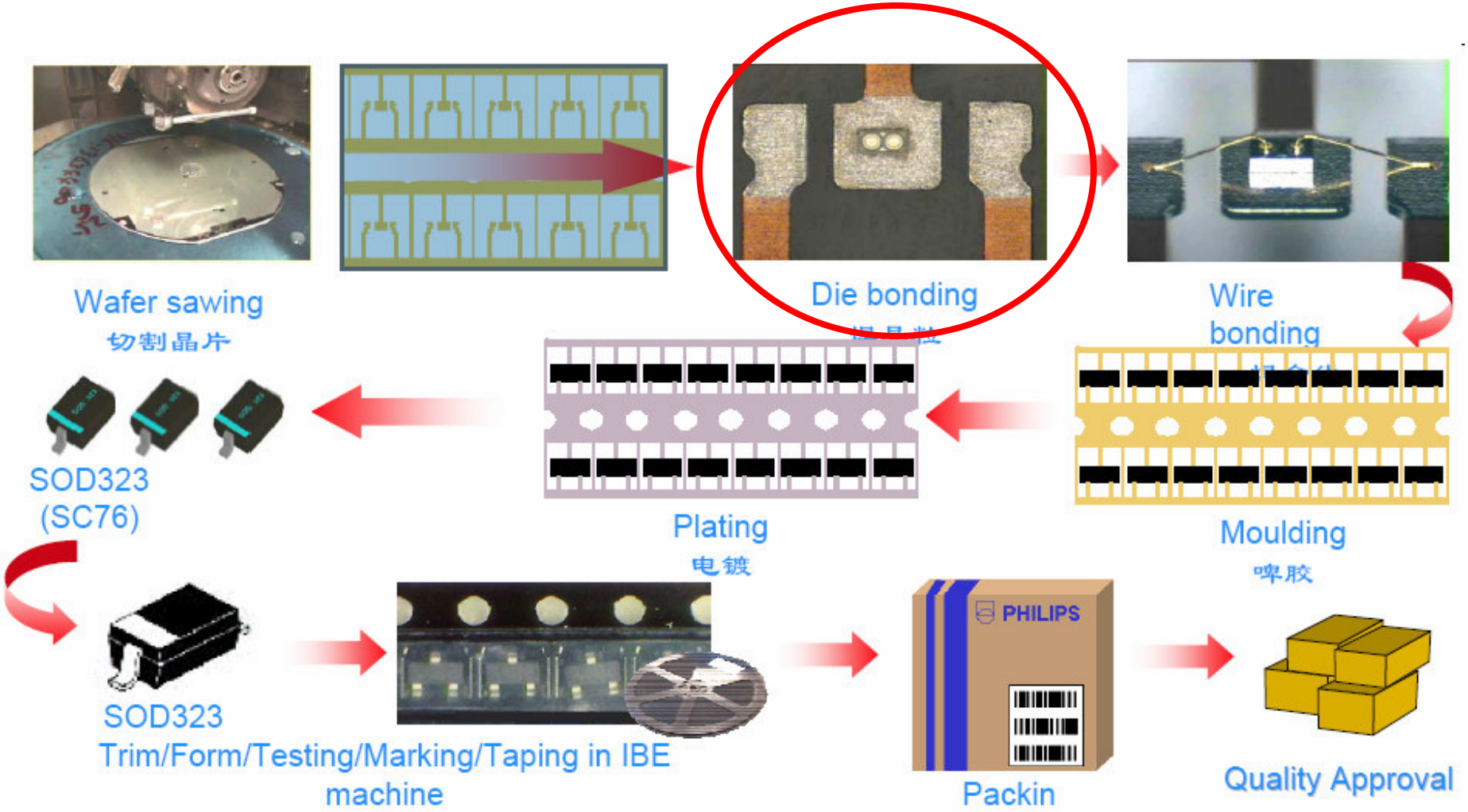
Function: ensure that leads can reach the printed circuit board

- Process:
  - a dejunk
  - b dambar cutting
  - c form (leadshapes)
  - d knock out





Process Summary



Process of High Pb solder usage

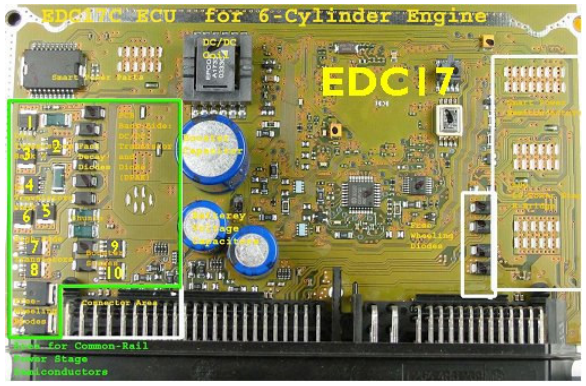
Die attach/ Die bond

Die Attach

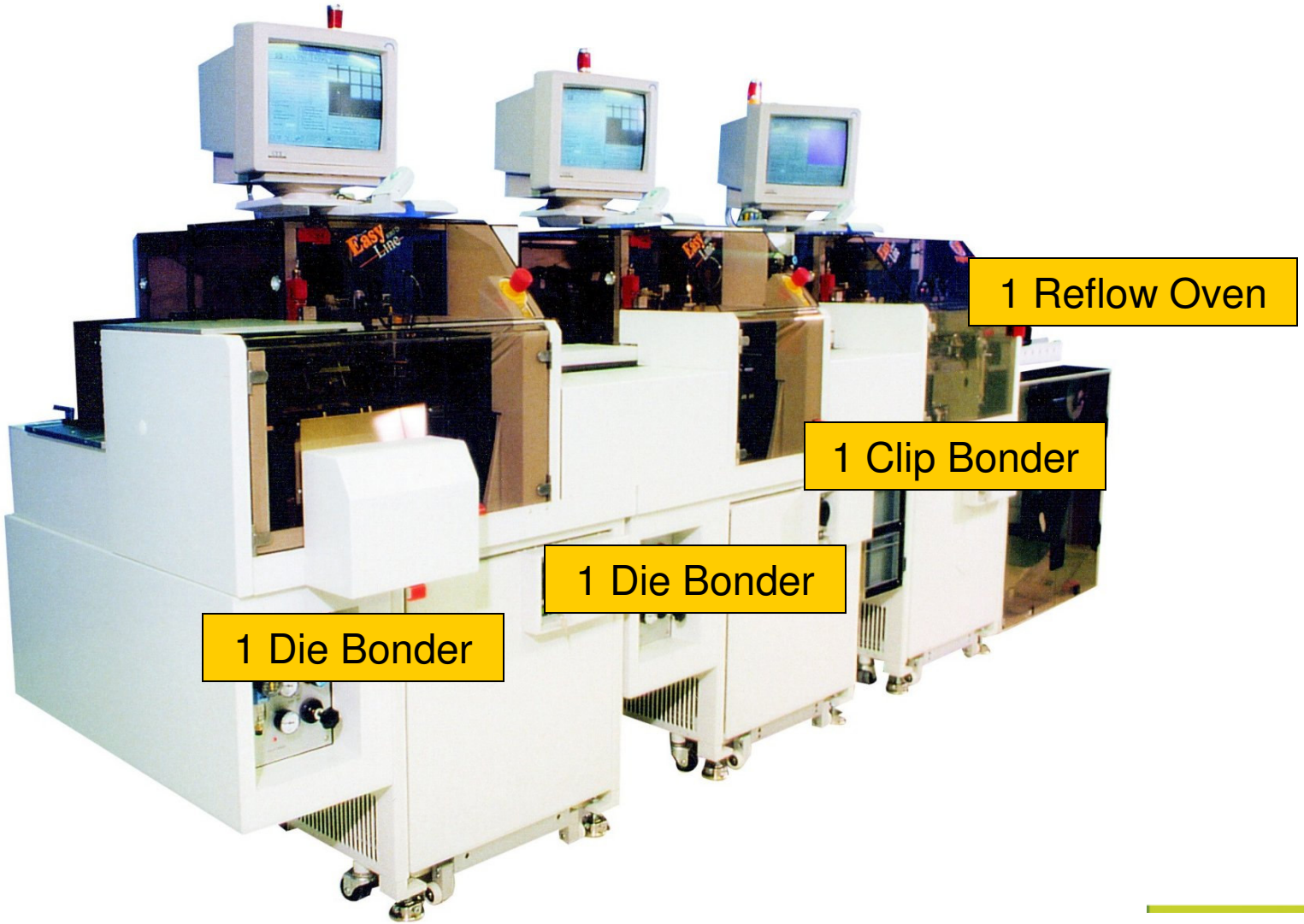
- Multiple Options available
- Within IC manufacturing mainstream is Epoxy die attach
  - Ag particle filled Epoxy
- However, for Power Devices Solder is used
  - heat capacity of connection is important
- Discrete Semiconductors with 'small' dies also use Solder die attach
  - Small effect of CTE mismatch between die and leadframe

Applications with solder die bond

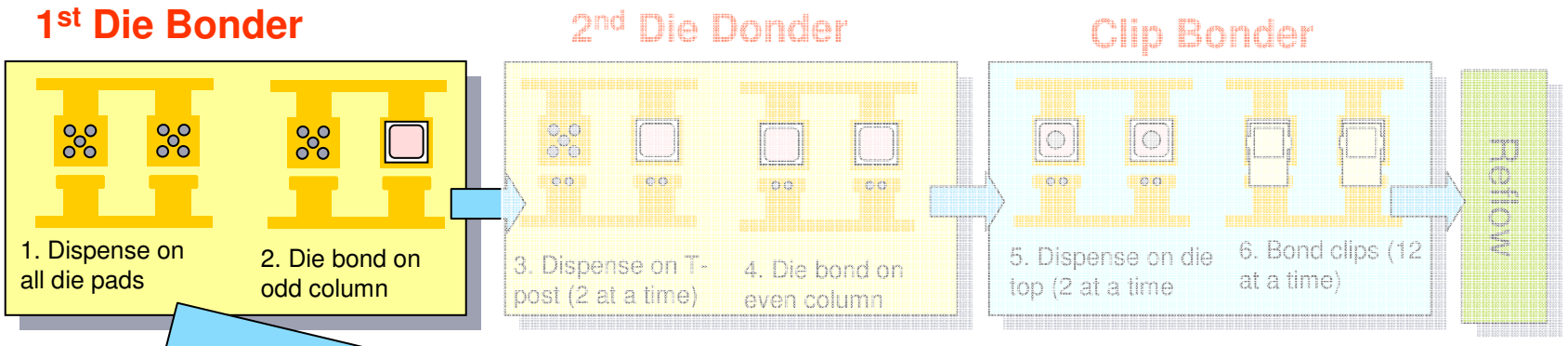
- DC/DC Converters
- Notebook computers
- Desktops and servers
- High Frequency Applications
- Electronic Diesel Control for automotive



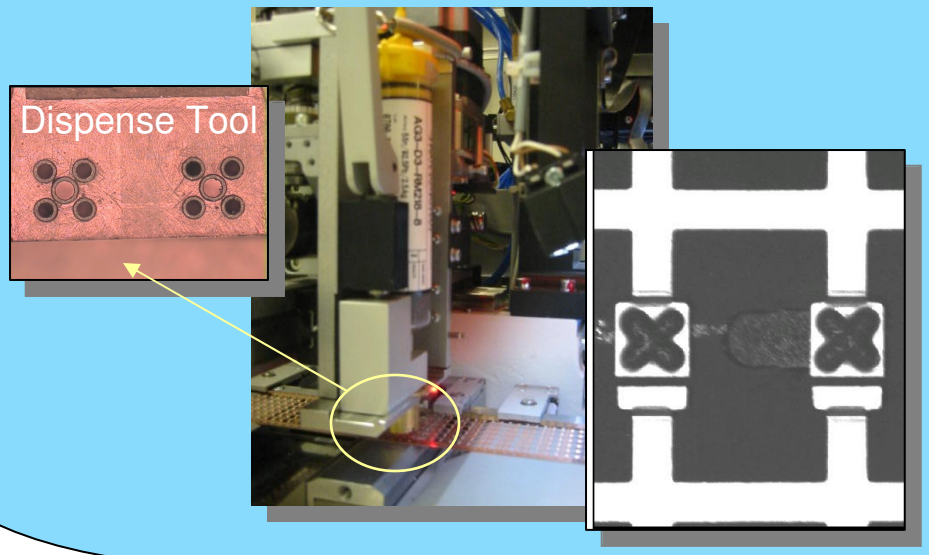
Die Bond Process Example: Equipment



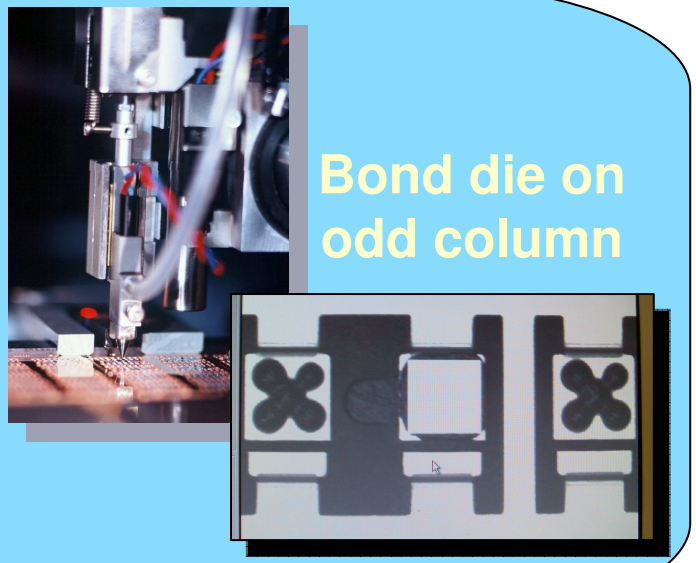
Process Flow (1)



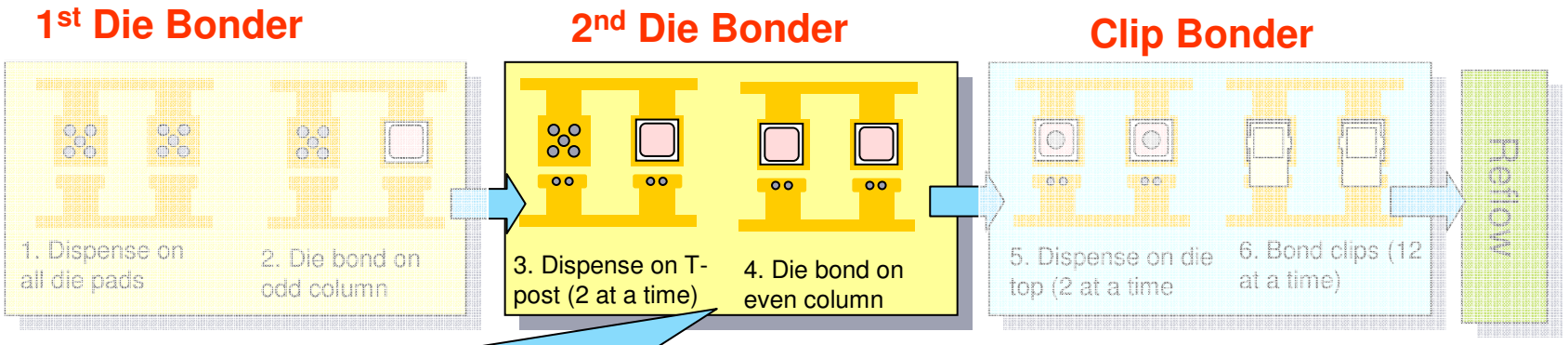
Dispense on LF Pad

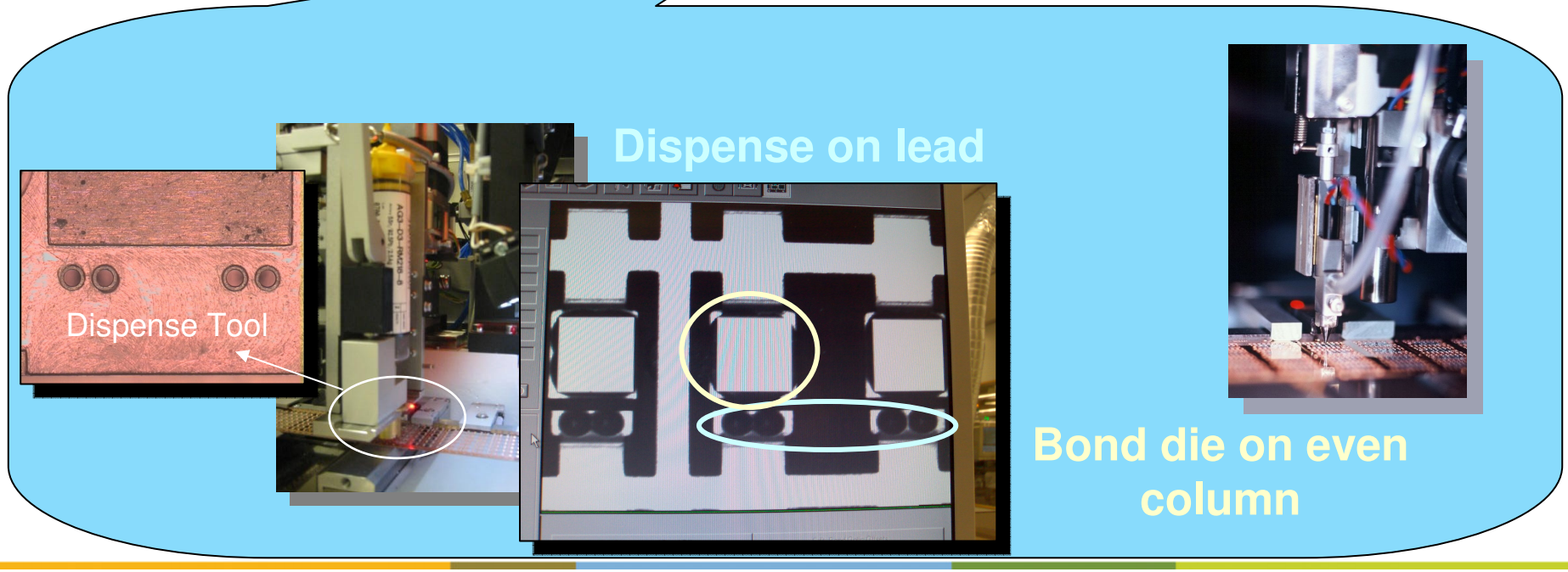


Bond die on odd column

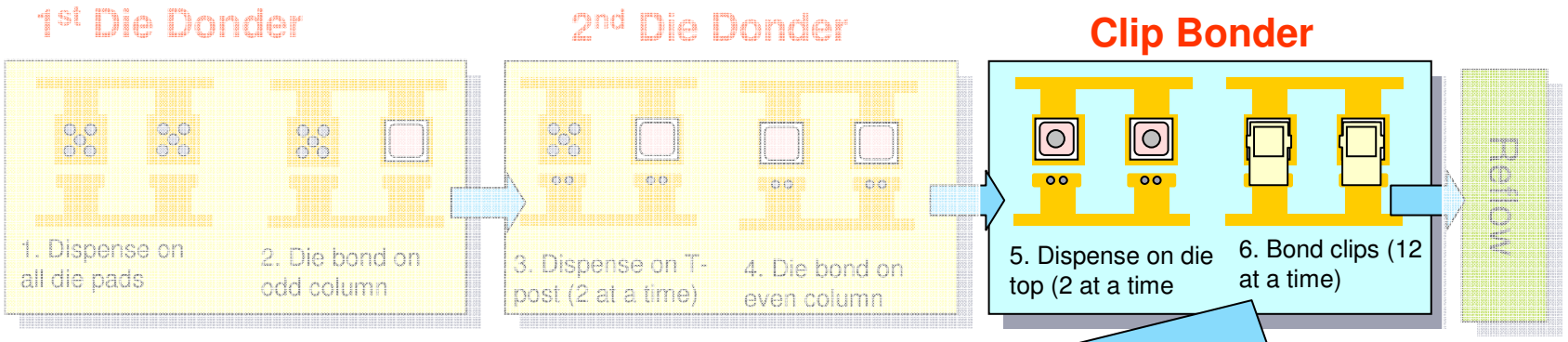


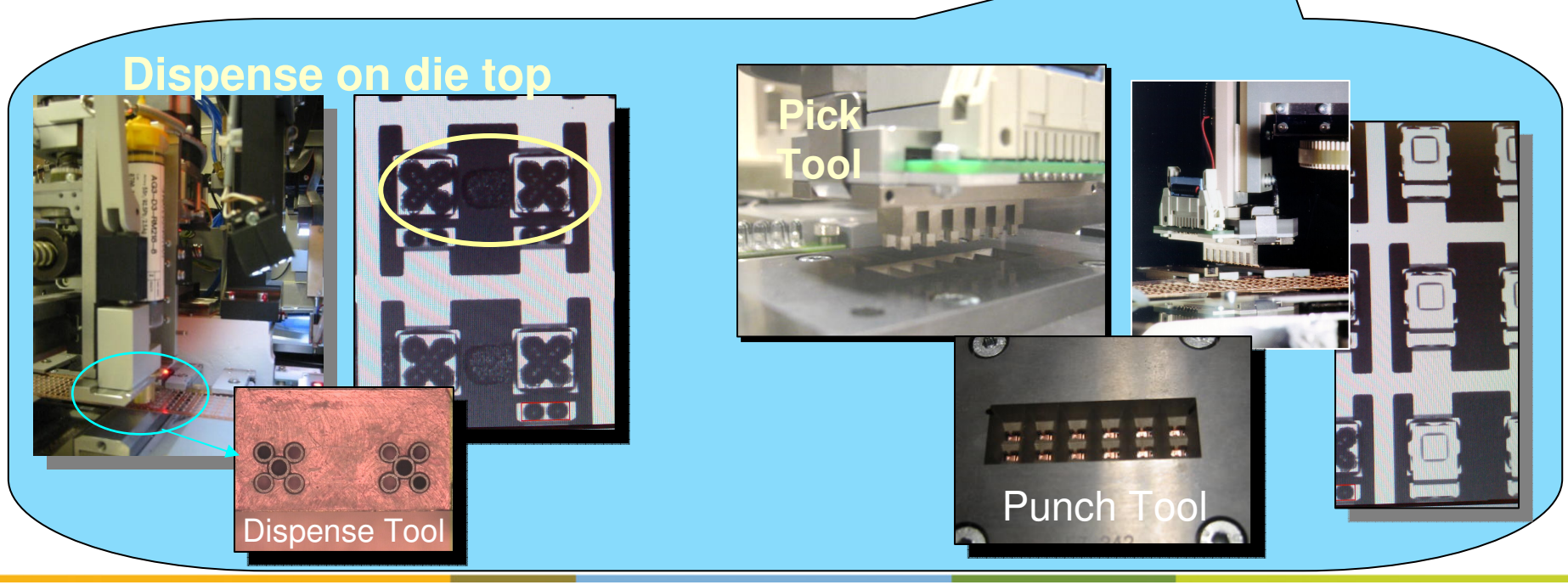
Process Flow (2)



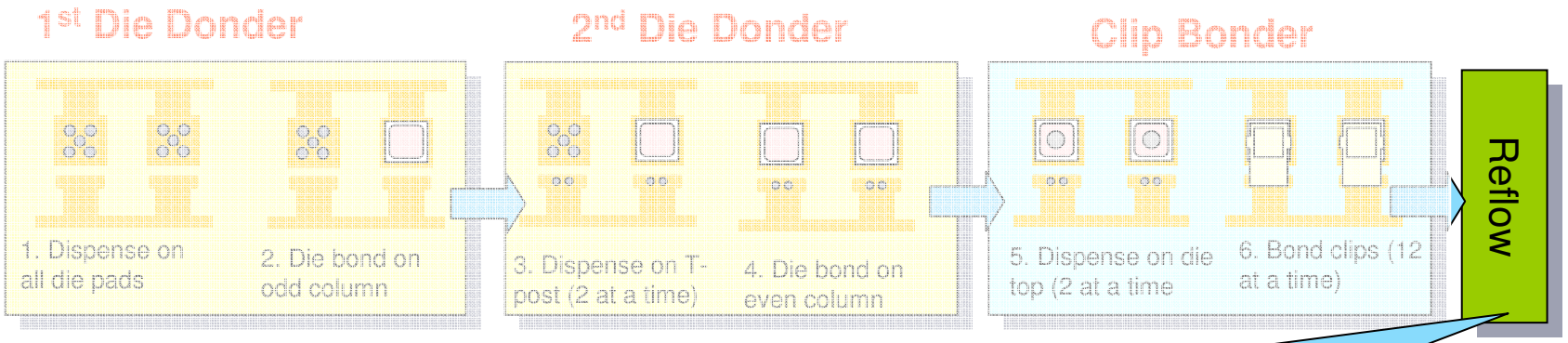


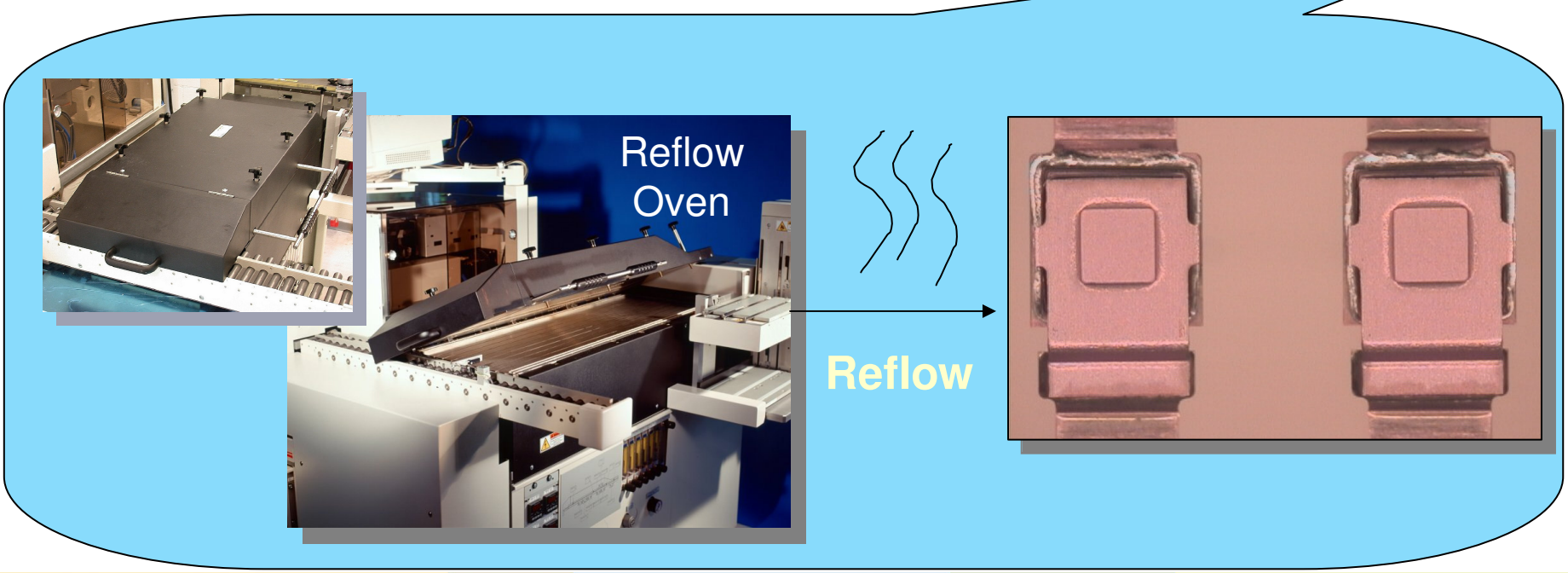
Process Flow (3)



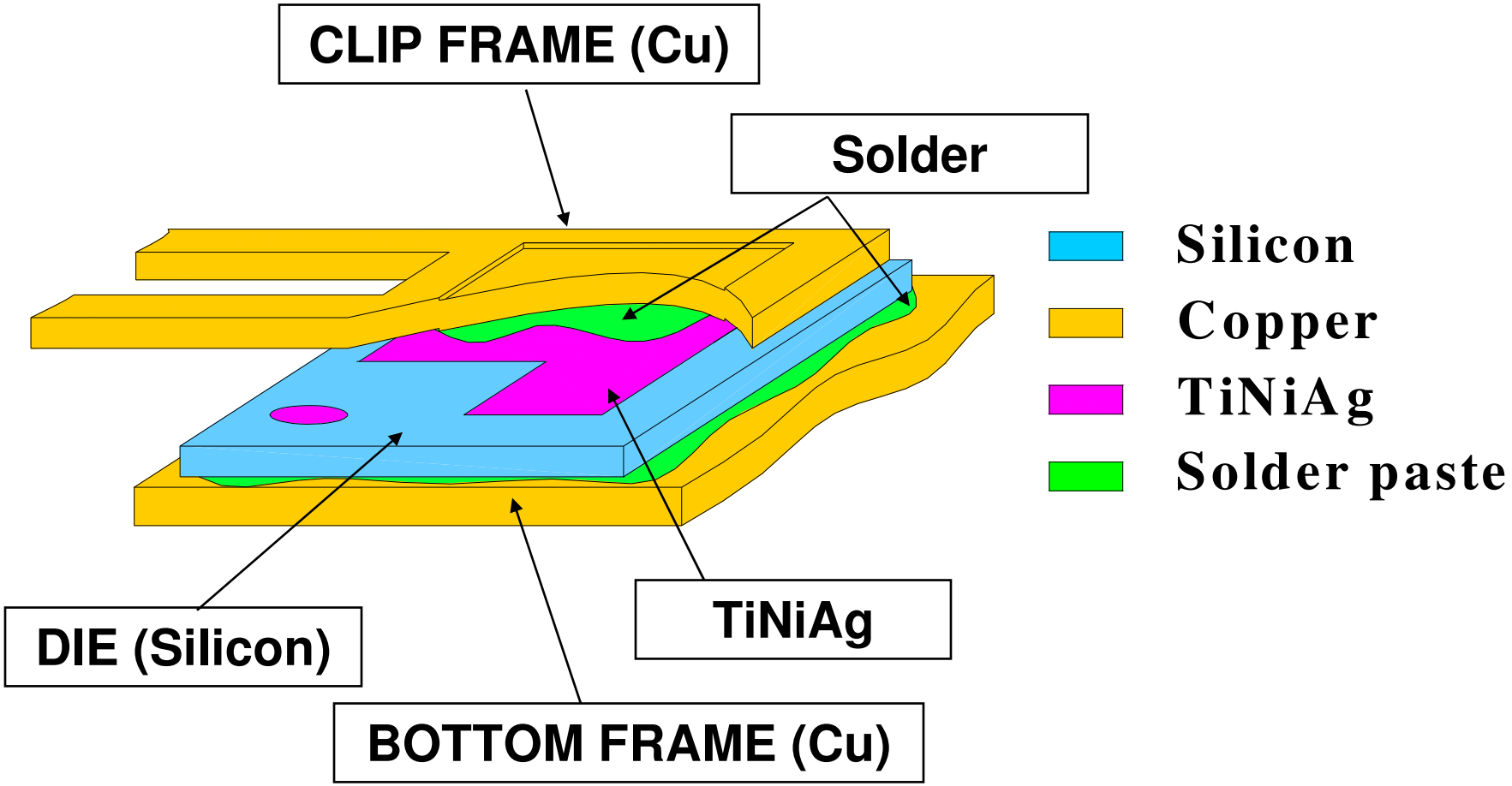


Process Flow (4)





Internal Package Construction (discrete device)

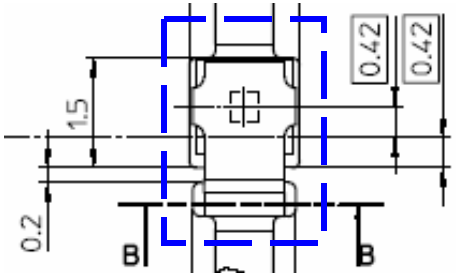


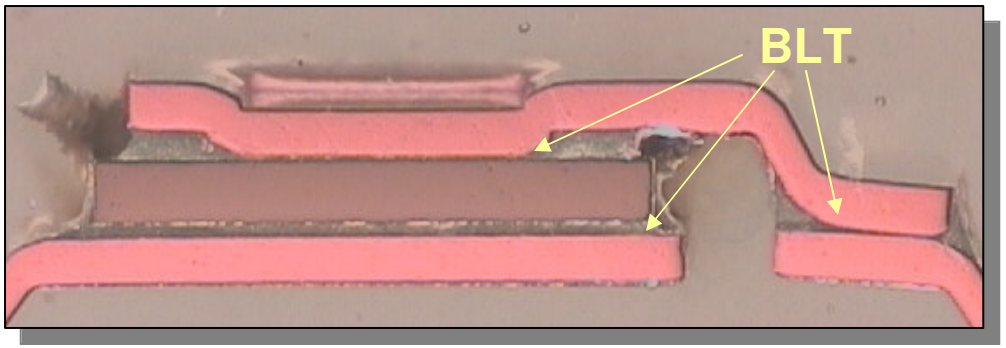
Specifications

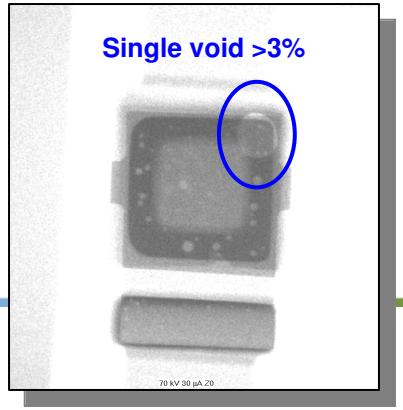
- Before reflow
  - Die placement +/-50um
  - Die rotation +/-2deg
  - Clip placement +/-50um
  - Clip rotation +/-3deg

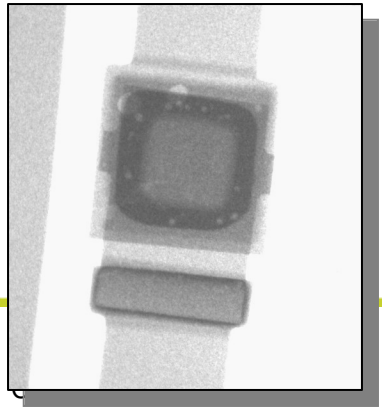
- After reflow
  - Die placement +/-100um
  - Die rotation +/-5deg
  - Clip placement +/-100um
  - Clip rotation +/-5deg
  - Clip tilt <2.5deg
  - **BLT >15um**
  - **Solder Coverage 100%**
  - **Void**
    - **Single void < 3%**
    - **Total void <5%**

Clip placement



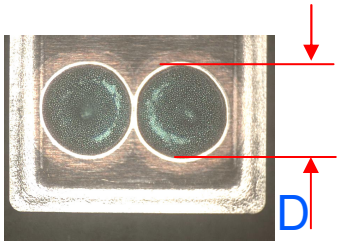






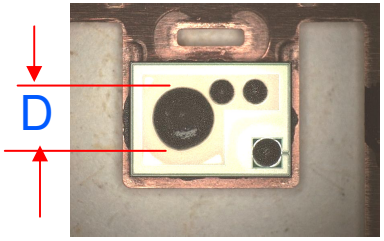
Dimensional Example (3.9 x 2.8mm die size)

Leadframe



- **Diameter should be within 1.6±0.1mm.**
- **Bond Line Thickness will be 40±10um**

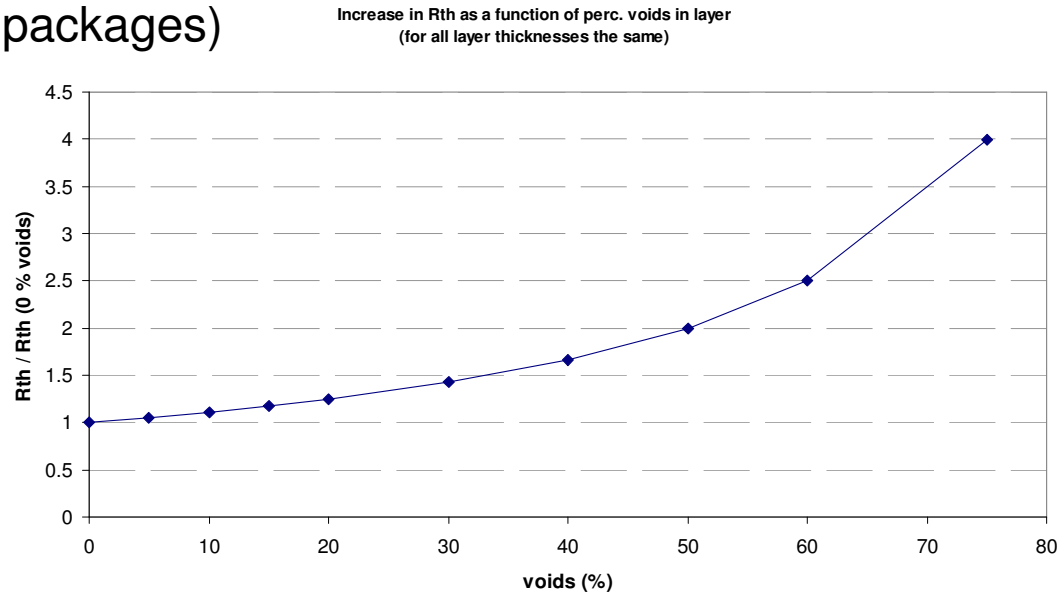
Die



- **Diameter should be within 1.36±0.1mm.**
- **Source Bond Line Thickness will be 20±5um**

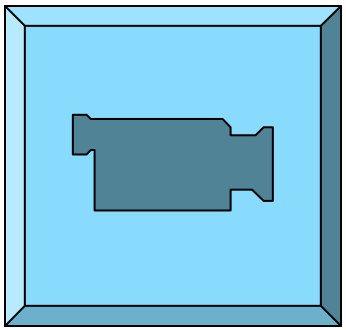
Remarks

- In this example solder paste was used, not always applicable
- Flux in the paste can have a corrosive action on die top surface
- Flux also causes voiding, which is undesirable in case the die attach is used as a thermal conductive pad (power packages)



- In cases where no flux can be used die attach is doen under protective atmosphere (forming gas)

Die attach Process in action



Materials used with High Pb solder

Bonding metals

Leadframe:

1. Cu- alloy (possibly Ag spot plated)
2. NiFe

Die backside:

1. TiNiAg
2. NAT (AuGe/Ni/Ti/Au)

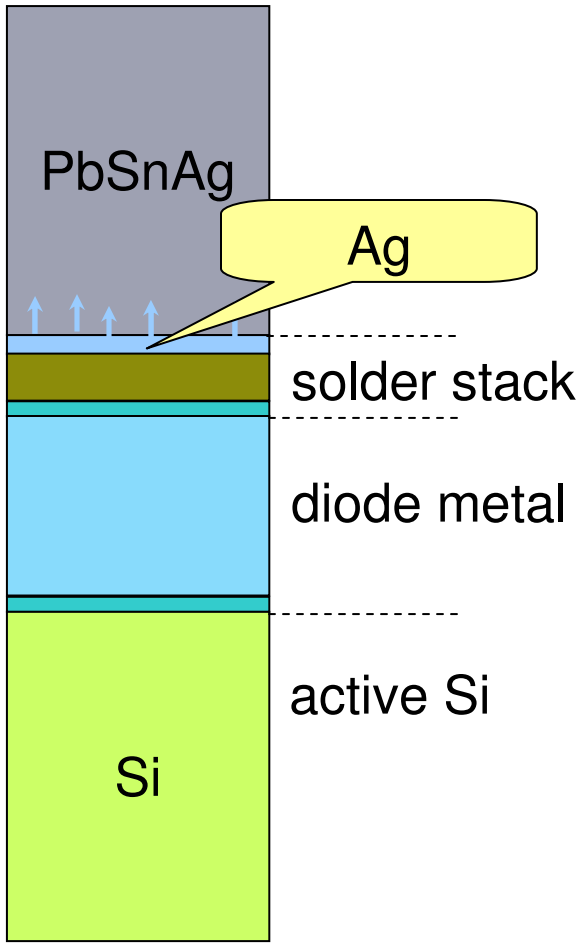
Common leadframe materials and properties

ALLOY	COMPOSITION	DENSITY	THERMAL EXPANSION	TEMPER	THERMAL CONDUCTIVITY	ELECTRICAL RESTIVITY	ELECTRICAL CONDUCTIVITY	ELASTIC MODULUS	TENSILE STRENGTH	YIELD STRENGTH	ELONGATION	HARDNESS
	NOMINAL %	g/cc	1/°C		W/m°C 20°C - 200°C	u ohm*cm	% IACS	Gpa	MPa	Mpa (NOMINAL)	% in 50mm	HV
ALLOY42	Fe Ni 41 Mn .8 Co .5	8.1	4.3	½ Hard	11	66.3	3%	156	620 - 724		3%	
				¼ Hard	11	66.3	3%	156	690 - 828		1%	
C151	Cu Zr 0.1	8.94	17	¼ Hard SOJ & PLCC	360	1.9	95%	120.7	325-385	345	5% Min	100 - 120
C194	Cu Fe 2.35 P 0.03 Zn 0.12	8.92	17.1	Hard SOIC & PLCC	277	2.54	60%	120.7	415-480	415	4% Min	125 - 145
				Spring(RA) DIP	277	2.54	60%	120.7	480-525	435	4% -8%	140 - 155
				ExSpring(RA) DIP & QFP	277	2.54	60%	120.7	530-570	470	5% Min	150 - 165
C7025	Cu Ni 3.0 Si 0.65 Mg 0.15	8.8	17.2	TR02 QFP & TSSOP	170	4.3	45%	131	605 Min.	550-655	6% Min	180 - 220
				TR04 Fine pitch w/ thinner L/F material	133	4.9	35%	131	790 Min	750-850	1% Nom	250 Nom
EFTEC-3 CDA14410	Cu Sn 0.15	8.9	17.3	¼ Hard	360	---	90%	118	216-294	---	25% Min	65 - 100
				½ Hard	360	---	90%	118	255-333	---	15% Min	75 -110
				Full Hard	360	---	90%	118	314-392	---	5% Min	95 - 130
EFTEC-64T CDA18040	Cu Cr 0.3 Sn 0.25 Zn 0.2	8.9	17	¼ Hard	301	---	75%	127	---	---	---	----
				½ Hard	301	---	75%	127	490-588	---	10% Min	160 - 195
				Full Hard	301	---	75%	127	539-637	---	5% Min	165 - 200

Function of Single Metals in Stack -Ag

Silver (Ag) 150nm

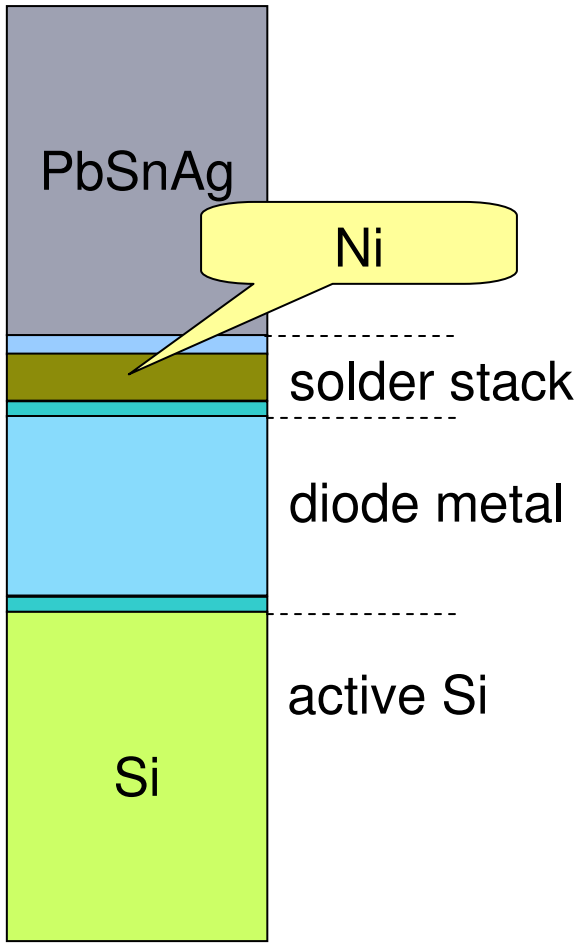
- Corrosion prevention of Nickel (Ni)
  - – Needs to be verified in detail
  - – Low thickness is preferable in wafer production
    - • Etch ability, wafer bow
- Ag has already saturation level in solder paste
  - PbSnAg
  - – Some competitors use thicker Ag
  - – Thickness can't be measured in cross section since Ag dissolves in the solder



Function of Single Metals in Stack -Ni

Nickel (Ni) 300nm

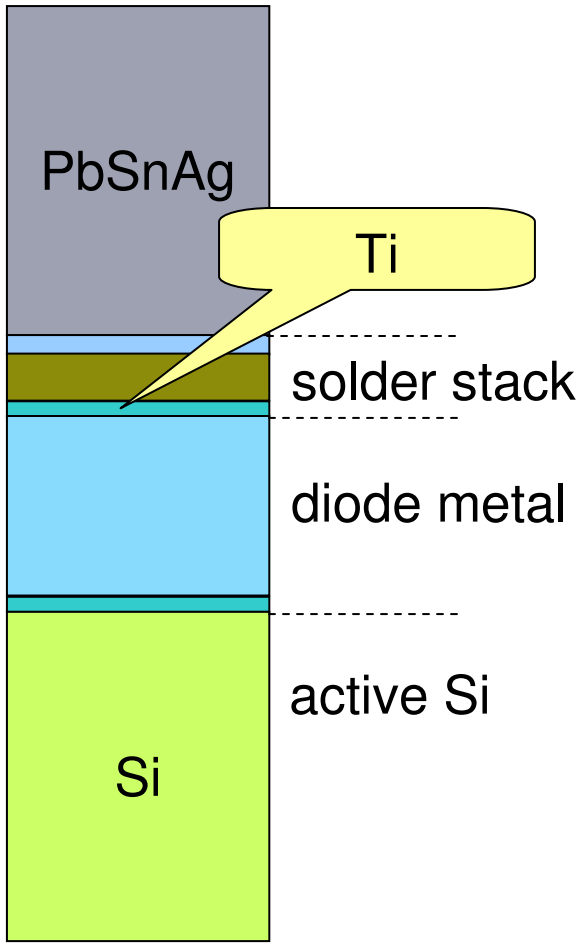
- Serves as metal to be soldered on
  - No intermetallic with lead (Pb) and limited in Ag
  - Only intermetallic with Tin (Sn) at Tm>794°C
- Prevents ions from diffusing into active area
  - Leakage currents in reverse condition



Function of Single Metals in Stack -Ti

Titanium (Ti) 100nm

- Implemented for good adhesion
  - On GOV (Si_3N_4) and on metal (here Al)
  - Reduces oxidation on Al (Al_2O_3)
  - Therefore improves serial resistance
  - Builds intermetallic with Ni and Al



Solder materials in use and properties

Within NXP the following materials are used for die attach solder

Material	Composition	Melting range (°C)	Density (g/cm^3)	CTE ($x10^{-6}/K$)	Thermal Cond. (W/m°K)	Electrical Cond. ($x10^{-6}/W/m$)	Elongation (%)	Young's modulus (GPa)	Tensile strength (Mpa)
J-alloy	**SnAg**25**Sb**10	228-395	7.8	19	55	6.5	1-4	23	80-120
PASN	**PbAg**3**Sn**5**Ni**0.2	301-309	11.04	-	34.6	-	15-20	5.5	~35
PAS	**PbAg**2.5**Sn**2	299-304	11.17	28.8	53	5.5	40-45	20	27-30
PAS	**PbAg**1.5**Sn**1	309	11.32	30	44	4.7	30-40	-	22-28

The Pb-free J-alloy can not always be used……

Solder materials on the market

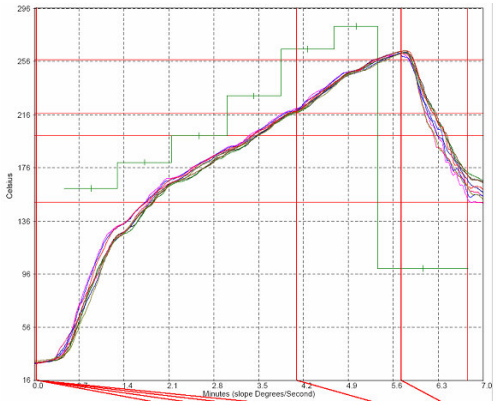
Alloy	Solidus	Liquidus	Common Name	Differentiating Property
Sn5, Pb95	308°C	312°C	Sn5	High-temp solder
Sn10, Pb88, Ag2	267°C	290°C	10-88-2, Sn10	High-temp solder
Sn5, Pb92.5, Ag2.5	287°C	296°C	151	High-temp solder
Sn5, Pb85, Sb10	245°C	255°C		Creep resistant
Sn65, Ag25, Sb10	233°C	233°C	J-Alloy	Pb-free, high tensile strength
Sn95, Sb5	235°C	240°C	Sb5	Pb-free
Au80, Sn20	280°C	280°C	AuSn Eutectic	Pb-free, eutectic
Sn2, Pb95.5, Ag2.5	299°C	304°C		Low Sn
Sn1, Pb97.5, Ag1.5	309°C	309°C		Low Sn, eutectic
Sn96.5, Ag3.5	221°C	221°C	Sn96	Eutectic
60Pb, 40In	197°C	231°C		In adds fatigue resistance
75Pb, 25In	240°C	260°C		In adds fatigue resistance
81Pb, 19In	260°C	275°C		In adds fatigue resistance
92.5Pb, 5In, 2.5Ag	300°C	310°C		In adds fatigue resistance
Sn10, Pb90	275°C	302°C		High-temp solder

→ Pb-free alloys are available!!!!!! However…….

Available Alternatives

- AuSn Eutect Cost!!!
  - Too expensive to use!
  - Environmental impact?

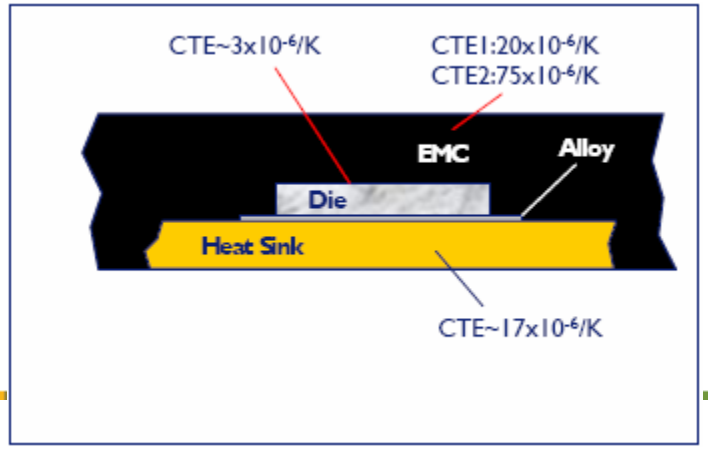
- Sn based J-alloy / SnSb5/SnAg3.5
  - Too low melting point
  - Pb-free soldering moved peak temperature during board assembly to 260 °C



Requirements for Alternative Die Attach (1)

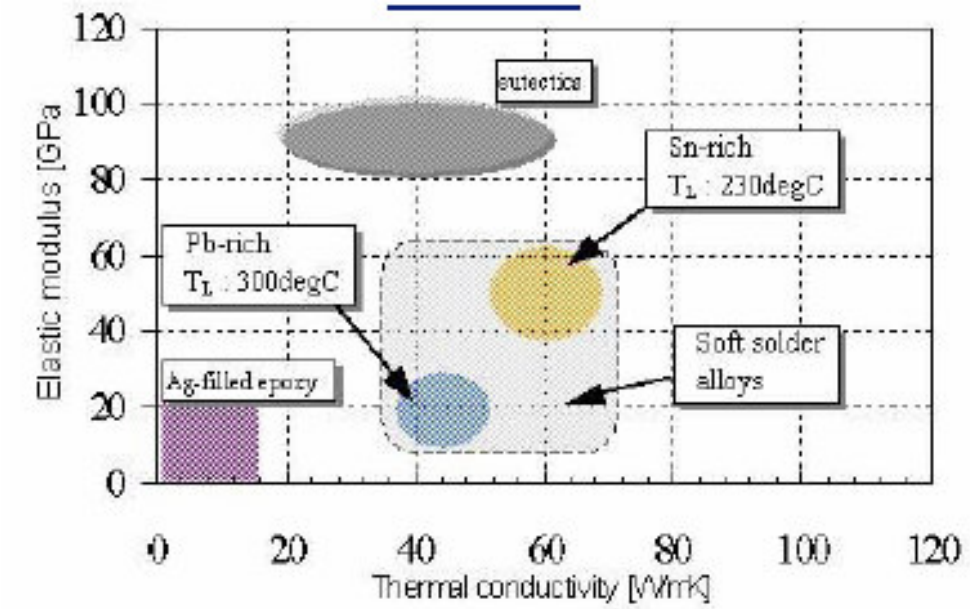
Some of the required properties are mentioned below

- Non toxic
- Good mechanical strength (At least up to 150°C)
- Process temperature that will not affect the die function (<400 °C)
- Thermally stable to > 270 °C
- Stress absorption from thermal expansion mismatch between the die and substrate



Requirements for Alternative Die Attach (2)

- Joint fatigue resistance - mechanical and thermal
- Electrical/thermal conduction
- Chemical inertness with low outgassing
- Ability to automate current process



New Developments

- ZnAl
  - Corrosion issue
  - http://www.oerlikon.com/ecomaXL/index.php?site=ESEC_EN_tp_soft_solder
- BiAg
  - Low thermal conductivity?
  - www.oerlikon.com/ecomaXL/get_blob.php?name=leadfree_paper_semi_china_2002_02.pdf&download=1 -
- CuSn
  - Solidification, process parameters
  - http://techon.nikkeibp.co.jp/english/NEWS_EN/20080201/146818/

Thank You for your Attention