Seminar Hora Informaticae **Institute of Computer Science, Prague**

Tuesday, June 13, 2023, 14.00 – 15.30 (2 - 3:30 PM) CEST

Meeting room 318, Address: Pod Vodárenskou věží 2, Prague 8

ZOOM: https://cesnet.zoom.us/j/95478234977?pwd=dXoyekFHbDJ0MkNrTjVVS3F2STZqUT09

Meeting ID: 954 7823 4977 , Passcode: 712564

Jiří Kadlec, Department of Signal processing, UTIA, CAS:

HW Accelerated AI Inference and Fast, Recursive QR System Identification.

We will explain design, implementation and performance of HW accelerated AI inference with 8-bit, fixed point, neural networks for object detection (resnet50) and face detection (dense-box_640_360) on System-on-Chip (SoC) AMD-Xilinx Zynq UltraScale+ device. It is 4-core ARM A53 64bit processor with on-chip programmable logic [1]. We will also explain implementation and performance of HW accelerated, fast, recursive, adaptive system identification QR Lattice algorithms. Algorithms are implemented as pipelined systolic arrays on our floating point FP32 SIMD data processing engines (DPUs) on Zynq UltraScale+ device [2].

References:

[1] Zdeněk Pohl, Lukáš Kohout, Jiří Kadlec, Xilinx Vitis AI 'facedetect' Demo on Trenz Electronic board TE0808 SoM + TEBF0808 Carrier. https://zs.utia.cas.cz/index.php?ids=results&id=facedetect https://zs.utia.cas.cz/results/facedetect/facedetect_demo_te0808_rev01.pdf

[2]Ing. Raissa Likhonina, PhD. Fast Bayesian Algorithms for FPGA Platforms. PhD thesis, CTU prague. https://asep.lib.cas.cz/arl-cav/cs/detail-cav_un_epca-0566001-Rychle-algoritmy-Bayesovskeho-rozhodovani-pro-FPGA-platformy,http://library.utia.cas.cz/separaty/2022/ZS/likhonina-566001.pdf

---

Jiří Kadlec (https://zs.utia.cas.cz/index.php?ids=staff&id=kadlec) is responsible for the Department of Signal processing in UTIA AV CR v.v.i. We focus on research, development and implementation of advanced digital signal and image processing algorithms, mainly in the fields of audio processing and scene analysis (image segmentation, motion detection, object detection). We build on our experience with the Bayesian approach to recursive identification of linear systems with time variable parameters.

Our target platforms are Field-Programmable Gate Arrays (FPGAs). We are focused mostly on embedded SoC solutions based on AMD-Xilinx Zynq and ZynqUltrascale+ devices programmed by AMD-Xilinx Vivado and Vitis tools. We also use Matlab/Simulink and OpenCL, OpenCV frameworks to specify, model and verify algorithms which we subsequently convert and synthesize the programmable logic. We study features which result in fast execution, small memory footprint, small chip area and low power consumption. This is achieved by modifying of DSP algorithms and by exploiting advanced architectural properties of embedded edge devices.

Our department is participating mainly in EU RTD projects supported by the ECSEL/KDT Joint Undertaking.

https://zs.utia.cas.cz/index.php?ids=news

HORA INFORMATICAE (meaning: TIME FOR INFORMATICS) is a broad-spectrum scientific seminar devoted to all core areas of computer science and its interdisciplinary interfaces with other sciences and applied domains. Original contributions addressing classical and emerging topics are welcome. Founded by Jiří Wiedermann, the seminar is running since 1994 at the Institute of Computer Science of the Czech Academy of Sciences in Prague.

https://www.cs.cas.cz/horainf